Amendment to Claims

1-21 (canceled).

22 (currently amended). A method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions of a first conductivity type in a semiconductor substrate and having a channel region in the semiconductor substrate between the source/drain regions, the method comprising:

forming a first conductive gate comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and

forming a floating gate overlying a portion of the channel region.

23 (original). The method of Claim 22 wherein the first conductive gate is a gate of a buried channel transistor.

24 (original). The method of Claim 22 wherein the channel region comprises a surface region underlying the first conductive gate and having a lower net dopant concentration of the second conductivity type than a region immediately below the surface region.

25 (original). The method of Claim 24 wherein the surface region is at most 0.2 μm deep.

26 (currently amended). The method of Claim [[1]] 22 further comprising implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to lie below the first conductive gate.

27 (original). The method of Claim 26 wherein the surface region is at most 0.2 μm deep.

28 (original). The method of Claim 22 wherein the channel region has the second conductivity type.

29 (currently amended). The method of Claim 22 wherein the first conductive gate is to turn on the underlying portion of the channel region ~~portion~~ to provide access to the nonvolatile memory cell.

30 (currently amended). The method of Claim 22 wherein the floating gate is one of two floating gates of the nonvolatile memory cell, each floating gate overlying a portion of the channel region.

31 (original). The method of Claim 22 wherein the first conductivity type is type N.

32 (original). The method of Claim 22 wherein the first conductivity type is type P.

33 (currently amended). [[An]] A method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions of a first conductivity type in a semiconductor substrate and having a channel region in the substrate between the source/drain regions, the method comprising:

forming a first conductive gate overlying a portion of the channel region; and

forming a floating gate overlying a portion of the channel region;

wherein the first conductive gate is a gate of a buried channel transistor.

34 (original). The method of Claim 33 wherein the channel region comprises a surface region underlying the first conductive gate and having a lower net dopant concentration of the second conductivity type than a region immediately below the surface region.

35 (original). The method of Claim 34 wherein the surface region is at most 0.2 μm deep.

36 (original). The method of Claim 33 further comprising implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to lie below the first conductive gate.

37 (original). The method of Claim 36 wherein the surface region is at most 0.2 μm deep.

38 (original). The method of Claim 33 wherein the channel region has the second conductivity type.

39 (original). The method of Claim 33 wherein the first conductive gate is to turn on the underlying portion of the channel portion to provide access to the memory cell.

40 (original). The method of Claim 33 wherein the floating gate is one of two floating gates of the memory cell, each floating gate overlying a portion of the channel region.

41 (original). The method of Claim 33 wherein the first conductivity type is type N.

42 (original). The method of Claim 33 wherein the first conductivity type is type P.